## REMARKS

### Claim Rejections – 35 U.S.C. §103

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Abramovici et al. (US 6,108,806), in view of Andrews et al. (US 6,064,225).

For a §103 obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. MPEP 2143.

Amended Claim 1 recites a method of testing the routing circuitry in a field programmable gate array (FPGA), wherein the method comprises "providing a global control signal to said first end of one of said first set and said second set of tracks, said global control signal turns on all interconnect elements of said one of said first set and said second set of tracks simultaneously ...."

Neither Abramovici nor Andrews disclose providing a global control signal to the first end of one of a first set and a second set of tracks, wherein the signal turns on *all interconnect elements* of the one of first and second set of tracks *simultaneously*, as recited in Claim 1. Andrews does not mention a global control signal at all, nor does Examiner assert that it does.

At the bottom of Page 4 of the Final Office Action dated April 19, 2005, Examiner does argue that Abramovici teaches "that the FPGA is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test ...." However, Abramovici fails to teach that the configuration data

*simultaneously* turns on *all interconnect elements* of a set of tracks. Abramovici merely teaches "retrieving a BIST configuration from the configuration storage of the test controller and loading it into the FPGA." (Col. 4, lines 53-55). There is no detailed discussion of how this configuration data affects the FPGA. Applicant cannot find, nor has Examiner cited, any mention in Abramovici of global control signals *simultaneously* turning on *all interconnect elements* of a set of tracks.

Since neither Abramovici nor Andrews individually disclose providing a global control signal to the first end of one of a first set and a second set of tracks, wherein the signal turns on all interconnect elements of the one of first and second set of tracks simultaneously, they cannot teach this element in combination. Examiner has failed to establish that all elements of the invention are disclosed in the prior art. Furthermore, since the cited prior art does not disclose this claim limitation, there is clearly no suggestion or incentive that would motivate one skilled in the art to modify or combine the prior art to include this limitation.

Therefore, Applicant respectfully submits that Claim 1 is non-obvious over Abramovici in view of Andrews, and that Claim 1 is currently in condition for allowance.

The same arguments made above with respect to the patentability of Claim 1 are applicable to the patentability of Claims 2 and 3 as well. Applicant respectfully submits that Claims 2 and 3 are currently in condition for allowance.

Reconsideration and withdrawal of this rejection is respectfully requested.

Claims 4 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Abramovici, in view of Wells et al. (US 6,651,238), in further view of Andrews.

The same arguments made above with respect to the patentability of Claim 1 are applicable to the patentability of Claim 4 as well.

Since Claim 5 depends from Claim 4, Applicant respectfully submits that Claim 5 is also patentable as it contains the same limitations as Claim 4.

Applicant respectfully submits that Claims 4 and 5 are currently in condition for allowance. Reconsideration and withdrawal of this rejection is respectfully requested.

Amendment to Claim 1

Applicant respectfully submits that no new matter has been introduced by the amendment to Claim 1.

If the Examiner has any questions regarding this application, the Examiner may telephone the undersigned at 775-586-9500.

Respectfully submitted,
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